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Call-for-Participation

2013 Pacific-Rim Dependable Computing

December 4-6, 2013

The 2013 Pacific-Rim Dependable Computing (PRDC'2013) is open to the general public for registration. As the main event in the Pacific area that is devoted to dependable and fault-tolerant computing, the nineteenth symposium will take place in December 4 to 6 in Vancouver, Canada.

The two-and-half day program will feature two keynote speeches and over fifty technical presentations that encompass many dimensions of dependability and fault tolerance, including fundamental theoretical

approaches, practical experimental projects, and commercial components and systems.

One keynote speech will be given by Prof. Tadayoshi Kohno from University of Washington, titled, "Computer Security and Everyday Objects: Case Studies with Medical Devices, Robots, and Automobiles".

The other one will be given by Dr. Kenny Gross of Oracle, titled, "Comprehensive Prognostics for Enhanced Dependability of Integrated Hardware/Software Enterprise Servers and Clusters".

More details about the conference can be found at
<http://prdc.dependability.org/2013>.

On-line registration can be made at
<http://prdc.dependability.org/2013/registration.html>.
We look forward to meeting you in Vancouver.

This symposium is not an IEEE sponsored event but will likely be of interest to many IEEE Vancouver members and is published here courtesy Joint Computer Society chair Sathish Gopalakrishnan



Marwan Krunz
University of Arizona

Security challenges and smart attacks in dynamic spectrum networks

Through opportunistic access to the radio spectrum, cognitive radio (CR) systems promise to salvage the underutilized spectrum and provide value-added services to wireless users. Despite the vast published literature in this area, harvesting the benefits of CRs in practical deployment scenarios still faces various security challenges.

In this talk, I will discuss several of these challenges and present potential solutions. Problems addressed include security issues caused by compromised nodes (a.k.a. “insider attacks”), in which an adversary seizes control of one of more legitimate CR nodes and exploits shared secrets/keys at these nodes to launch selective jamming attacks.

One such important attack that targets control-channel communications will be explored in detail. The problem of re-establishing opportunistic communications following a successful jamming attack and in the presence of dynamically available spectrum (so-called “rendezvous problem”) will also be discussed.

Speaker: Marwan Krunz is a professor of ECE and CS at the University of Arizona. He is also the UA site director for “Connection One”, a joint NSF/state/industry center that focuses on wireless communication systems and networks. In 2010, Dr. Krunz was a Visiting Chair of Excellence at the University of Carlos III de Madrid. He previously held other visiting research positions at INRIA, HP Labs, University of Paris VI, and US West Advanced Technologies. Dr. Krunz’s research interests lie in the fields of computer networking and wireless communications, with focus on distributed radio resource management in wireless and sensor networks; protocol design; and secure communications. He has published more than 200 journal articles and refereed conference papers.

He is an IEEE Fellow, an Arizona Engineering Faculty Fellow, and an IEEE Communications Society Distinguished Lecturer (2013 and 2014). He was the recipient of the 2012 IEEE Communications Society TCCC Outstanding Service Award. He received the National Science Foundation CAREER award (1998). He currently serves on the editorial board for the IEEE Transactions on Network and Service Management. Previously, he served on the editorial boards for the IEEE/ACM Transactions on Networking, the IEEE Transactions on Mobile Computing, the Computer Communications Journal, and the IEEE Communications Interactive Magazine. He was the general co-chair for the ACM WiSec 2012 Conference, and served as a TPC chair for various international conferences, including INFOCOM’04, SECON’05, and WoWMoM’06.

Monday 04 November

4:00 pm

Rm 418 - Macleod Bldg
2356 Main Mall, UBC

Information
Joint Communications
Chair Vincent Wong
vincentw@ece.ubc.ca



Jt. Chapter BT-02/COM-19/IT-12/ITS-38/PHO-36/VT-06



Michel Laberge
General Fusion

Monday 04 November
4:00-5:00 pm

TRIUMF Auditorium
4004 Wesbrook Mall
UBC

Information

Joint Applied Physics
Chair

Ahmed Hussein

Ahmed.Hussein@unbc.ca

Acoustically driven Magnetized Target Fusion at General Fusion

General Fusion (GF) is a private company developing nuclear fusion power generation. Most research on fusion is based on magnetic confinement or laser inertial confinement.

GF is exploring a less studied method called Magnetized Target Fusion (MTF). In MTF, a pre-formed low density, low temperature magnetically confined plasma is rapidly compressed to the higher density and temperature required to produce fusion energy. GF uses strong focussed shock waves in liquid metal generated by the impact of pneumatic pistons to compress the plasma, a very economical way of producing the very high energy density required for fusion.

In this talk we will describe GF MTF fusion power plant design and the progress achieved so far in our route to get to energy production.

Speaker: Dr. Michel Laberge is a physicist and engineer with widespread practical experience in plasma physics and modern plasma diagnostic techniques. He has extensive knowledge of the latest technologies related to electronics, computers, materials, lithography, optics and fabrication, and is experienced at designing and constructing test apparatuses to evaluate technical concepts.

Prior to establishing General Fusion, Michel spent nine years at Creo Products in Vancouver as a senior physicist and principal engineer. His roles included inventor, designer, main engineer, and scientific project leader on projects that resulted in more than \$1 billion worth of product sales.

Michel holds a B.Sc. and M.Sc. in physics from Laval University. In 1990, he earned his Ph.D. in physics from the University of British Columbia, and in 1991 completed a Post Doc. at L'ecole Polytechnique in Paris. In 1992, he completed another Post Doc. at the National Research Council in Ottawa. He has published numerous scientific papers.

A superconducting quantum annealing processor



Fabio Altomare
D-Wave Systems

Monday 25 November
4:00-5:00pm

TRIUMF Auditorium
4004 Wesbrook Mall
UBC

Information

Joint Applied Physics
Chair

Ahmed Hussein

Ahmed.Hussein@unbc.ca

D-Wave Systems has implemented a processor based on Quantum Annealing (QA), an algorithm for finding the ground state of a system of interacting spins. The motivation for this approach lies both in the observation that many high-value problems can be cast in this framework and, as importantly, that the physical requirements for implementing such an algorithm with a large number of spins can be realized with currently available technology in a semiconducting foundry.

In this talk I will present an overview of a Quantum Annealing algorithm based on an array of spins implemented as superconducting flux qubits. I will describe the qubits, how they are coupled, and the classical superconducting control circuitry which allows problems to be posed to the processor. Attention will also be devoted to the discussion of a

non-dissipative readout architecture, and its performance on a 512-qubit processor.

Speaker: Fabio Altomare received his Laurea from University of Pisa (Italy) where he studied transport in semiconducting heterostructures, and his Ph.D. from Purdue University, with a thesis on superconductivity in 1-dimensional nanowires.

He then worked as Postdoctoral Research Associate at Duke University, where he studied transport in dilute magnetic semiconductors, and at the National Institute of Standards and Technology in Boulder, where he studied superconducting qubits.

Since 2010, he has been working as an experimental physicist at D-Wave Systems, where he is involved in the practical implementation of an adiabatic quantum processor.





Doug Oucharek
Intel Corporation

Tuesday 26 November
5pm-6pm
Room E 103 (pending)
Okanagan College
1000 KLO Road
Kelowna Campus

Refreshments served

Information
IEEE Okanagan Chair
Youry Khmelevsky
youry@ieee.org

Clustered file systems for high performance computing and big data

The world of High Performance Computing (HPC) is one of vast numbers: tens of thousands of compute nodes clustered together, petabytes of shared storage, and kilometres of network cables. The demands HPC places upon storage systems is the most extreme of any other computing discipline.

In this talk, I will be outlining the specific requirements of HPC storage systems, and delve into the architecture of "Lustre": an open source parallel distributed file system used by the majority of the top 100 supercomputers. I will also be talking about the future of HPC file systems and how Big Data is adopting HPC file systems to improve performance.

Speaker : Doug Oucharek is the manager of the Lustre Core Development group at Intel. He was pulled into Intel as part of an acquisition of a startup supporting Lustre called "Whamcloud". Prior to working for Whamcloud, he spent over 25 years working on various networking products at several companies including Nortel, Motorola, IBM, HP, and Broadcom.

Doug works and lives in Naramata, BC, Canada.



Ian Horseman
TELUS Communications

Thursday 14 November
5pm-6pm

UBC Okanagan
Kelowna Campus
(Room TBA)

Refreshments served

Information
IEEE Okanagan Chair
Youry Khmelevsky
youry@ieee.org

The Evolution of telecommunications networks, and exploration of future topologies

Telecommunications networks have many inventors to credit with their creation, from Alexander Graham Bell, and Marconi, to innovators like John Watson. Their contributions mixed with a myriad of topology decisions combined to build a system that most of us rely on today. Have you ever wondered how they are built? Why technologies are chosen? Or, what variables will shape the network of the future? This talk will outline the genesis of telecommunications networks to date. It will examine the underlying causes for technology choices, and explore what holds change back. After doing so, the future state of networks can be projected. The talk will shed light on where we are going. It will give the audience a sense of why we need fibre to the home, and how we could get 1 Gbps connectivity to our phones.

Speaker Ian Horseman is currently an access planner for TELUS Communications Inc., where he is part of a team of specialists which determine what shape TELUS' network will take in the future. He has worked in telecommunications in a variety of roles for the past 11 years. While doing his undergrad (B.Eng '04) at Carleton University he was also a Technician for Bell Canada. After completing his degree he worked in a multi-discipline engineering role at Kenora Municipal Telephone Service (KMTS). He helped analyze and deploy wireline, mobility and fixed wireless networks within its serving area. In 2008, Ian moved to Kelowna, BC to work for TELUS. In his current role he has managed the deployment of telephone carrier systems, DSL network nodes (ADSL, and VDSL2), GPON and FTTx networks within BC. He is also a member of the November 2013 graduate cohort at UBC Okanagan, and will hold a Masters (M.Eng '13) focusing on small cell mobility networks and project management.



6TiSCH: IPv6 over IEEE802.15.4e

Qin Wang
University of Beijing

Friday 08 November
11:00 am to 12:30 pm

ASB 10900 (IRMACS
Presentation Studio),
Simon Fraser University,
Burnaby

Light refreshments
served.
Open to public.

Please register (aids our
estimating attendance)

Information
Circuits and Systems
Chair Ljiljana Trajkovic
ljilja@cs.sfu.ca

Low-power and Lossy Networks (LLNs) interconnect a possibly large number of resource-constrained nodes to form a wireless mesh network. The 6LoWPAN, ROLL and CoRE IETF Working Groups have defined protocols at various layers of the protocol stack, including an IPv6 adaptation layer, a routing protocol and a web transfer protocol. This protocol stack has been used with IEEE802.15.4 low-power radios.

The IEEE802.15.4e Timeslotted Channel Hopping (TSCH) is a recent amendment to the Medium Access Control (MAC) portion of the IEEE802.15.4 standard. TSCH is the emerging standard for industrial automation and process control LLNs, with a direct inheritance from WirelessHART and ISA100.11a.

Defining IPv6 over TSCH, 6TiSCH is a key to enable the further adoption of IPv6 in industrial standards and the convergence of Operational Technology (OT) with Information Technology (IT). The talk will give an overview about the on-going work 6TiSCH in IETF.

Speaker: Qin Wang is a professor of University of Science & Technology Beijing (USTB), China, and a visiting scholar in University of California at Berkeley, US. She received BS, MS, and Ph.D degree in Computer Science and Engineering from USTB in 1982, Peking University in 1985, and USTB in 1998, respectively.

She joined USTB in 1985, became full professor in 2000. She has been director of Micro-Architecture &

IC Laboratory in USTB since 2000. As visiting scientist (2005-2006) in EECS department of Cornell University, NY, and visiting researcher (2006-2007) in EECS department of Harvard University, Cambridge, MA, her research and contributions were on wireless sensor network technology and related power consumption modeling from both device and network system perspective.

Recent years, she has focused on low power wireless sensor networks and MPSoC (multiprocessor System-on-Chip) technology in communications and networking systems. She and her research team designed and deployed low power Large-Scale Wireless Sensor Networks applied to heavy industry including Anshan Iron and Steel Corp., a major iron and steel manufacturer in China. She has been involved in international wireless network standard development since 2007, including ISA100.11a, IEEE 802.15.4e, and industrial wireless standard WIA-PA proposed to IEC by China.



Optimization is the keyword in NanoCMOS



Ricardo Reis
UFRGS

Tuesday 12 November
2:00 pm to 3:30 pm

Rm 2020 Kaiser Bldg
2332 Main Mall
UBC

AND

Wednesday 13 November
2:00 pm to 3:30 pm

ASB 10900 (IRMACS
Presentation Studio),
Simon Fraser University,
Burnaby

Light refreshments
served.
Open to public.

Please register (aids our
estimating attendance)

Information

Circuits and Systems
Chair Ljiljana Trajkovic
ljilja@cs.sfu.ca

Power optimization in NanoCMOS must be observed in all levels of abstraction of the design flow and demands an important effort in optimization. As in NanoCMOS static power consumption is related to the amount of transistors, it is fundamental to change the design approach at physical level. It must be used an approach target to reduce the amount of transistors.

The traditional standard cell flow doesn't really take care of power minimization at physical level, because there is a limited number of logical functions in a cell library, as well a limited number of sizing versions. To really obtain an optimization at physical level, it is needed to allow the use of any possible logical function, by also using complex cells (Static CMOS complex gates . SCCG) that are not available in a cell library. To have a "freedom" in the logic design step, it is needed the use of an EDA set of tools to let the automatic design of any transistor network (even with a different number of P and N transistors). This approach can reduce the amount of transistors needed to implement a circuit, reducing the power consumption, mainly the leakage power.

The talk presents some examples and comparisons between the standard cell approach and the network of transistors approach. The flexibility of the approach can also let the designers to define layout parameters to cope with problems like tolerance to transient effects, yield improvement, printability and DFM. The designer can also manage the sizing of transistors to reduce power consumption, without compromising the clock frequency. High temperatures can reduce the reliability, so it is also important to reduce power consumption to improve reliability. The talk shows a new approach to reduce the amount of transistors by using complex gates and a new set of EDA tools to generate any transistor network. Some results show an important reduction on power consumption, improving also circuit reliability.

Speaker: Full Professor at Instituto de Informatica of the Universidade Federal do Rio Grande do Sul - UFRGS (professor since 1979). Electrical Engineering

from the UFRGS, Porto Alegre, Brazil, in 1978. Ph.D. degree from the Polytechnic Institute of Grenoble (INPG), France, January 1983. Member of the Microelectronics Committee of National Council for Scientific and Technological Development (CNPq). Former member of the Computer Science Committee of National Council for Scientific and Technological Development (CNPq), for two terms.

His primary research interests include Physical Design Automation and Methodologies, CAD tools, Circuits Tolerant to Radiation, VLSI Design Methodologies and Microelectronics Education. More than 350 hundred papers in journals and conferences proceedings. He is also author or co-author of several books. Invited speaker in several international conferences. Award as research of the year by the Science Foundation of Rio Grande do Sul, 2002. Silver Core award from IFIP. Research level 1A of the CNPq (Brazilian National Science Foundation). Head of several research projects. Past head of the Graduate Program in Microelectronics (2 terms) and of Computer Science Graduate Program at UFRGS (two terms). Professor and advisor at the Microelectronics and Computer Science Graduate Programs at UFRGS.

General Chair or Program Chair of several conferences like the IFIP/IEEE VLSI-SoC, IEEE ISVLSI, IEEE LASCAS, Symposium on Integrated Circuits and Systems Design (SBCCI) and Congress of the Brazilian Microelectronics Society (SBMIcro). Past President of the Brazilian Computer Society and Past Vice-President of the Brazilian Microelectronics Society. IEEE CASS Chapter Rio Grande do Sul Chair (since 2007). Vice-president of IEEE Circuits and Systems representing R9, for two terms, from 2008 to 2011. Member of the Editorial Board of IEEE Design&Test. Member of the Steering Committee of the following conferences: IFIP/IEEE VLSI-SoC, ICECS, LASCAS, NEWCAS, IEEE CASS Summer School, IEEE ISVLSI, SBCCI, IBERCHIP. Senior member of IEEE.



10th International Workshop on Complex Systems and Networks

SFU Harbour Centre
December 11-13, 2013

<http://iwcsn2013.eie.polyu.edu.hk/Home.html>

The International Workshop on Complex Systems and Networks (IWCSN) is a strongly interdisciplinary workshop intended to bring together mathematicians, physicists, biologists, social scientists, and engineers working on different aspects of network dynamics. The focus of IWCSN 2013 will continue to be devoted to the impact of network structure on systems dynamics. This area continues to be a hot research topic in all branches of science and technology.

The objectives are to provide opportunities for participants to learn about state-of-the-art research in various related yet disparate fields. We plan to have both tutorial talks and in-depth technical talks describing the latest research results and ongoing projects. Furthermore, these workshops provide opportunities for researchers and students from diverse disciplines to interact, find common ground, share results and insights, and foster collaboration.

Some of the questions that we have and would like to address in this workshop are: What are the universality properties of complex networks? For a particular application, what is the best complex network to deploy? How does the topology of the network influence various aspects of the underlying system? What can we learn from biological and social networks that may be useful in engineering networked systems and vice versa? What network models can be analyzed mathematically yet capture the salient features of the underlying ensemble systems? Can we build a taxonomy of complex network models that facilitates the identification of phenomena in ensemble systems?

The 2013 IWCSN will be divided into two main sections: theoretical works with a special focus on mathematical modeling and careful analytical studies a wide range of problems emanating from various applications in physics, chemistry, life sciences, engineering, and communications. There will be an opportunity for junior researchers and students to present their work including a session where researchers may pose interesting open questions.

Local organizer: The IRMACS Centre, Simon Fraser University

Sponsors: IEEE Circuits and Systems Society Centre for Chaos and Complex Networks, City University of Hong Kong, Hong Kong; IEEE Vancouver Section and IEEE Circuits and Systems Society joint Chapter of the Vancouver/Victoria Sections; Faculty of Applied Science and School of Engineering Science, Simon Fraser University

Inquiry: Ljiljana Trajkovic (Email: ljilja@sfu.ca)



An afternoon at the RIO Cinema

**Saturday 09 November
Noon to 04:00pm**

**1660 E Broadway
Vancouver**

**Information:
StevenMcClain@IEEE.ORG**



Come one, come all to the 2013 IEEE Vancouver's Social Event

We have booked the historic RIO theater for our own private party! We will meet at the RIO, and have (non-alcoholic) drinks and snacks while socializing and renewing friendships. Then we settle in for a movie that should appeal to us engineering types.

The movie is called "The Dish" and is based on a true story about a Australian radio telescope that was used to carry the television signal from the Apollo 11 moon walk. It is funny and entertaining and can be appreciated by young and old.

This event is open to all members and their families (children welcome) although the movie is rated PG13 for some mild language.

Ticket price is \$5 per person and will include a small popcorn and drink. Concession will be open if you want to buy more snacks. We would prefer that you register and pay beforehand but it will be possible to pay (cash) when you get there. Please register anyway so that we can plan accordingly.

Registration closes Nov 8.

Registration: https://meetings.vtools.ieee.org/meeting_registration/register/20687

12:00pm - doors open
Guests arrive and socialize
1:00pm - 3:30 film shows
4:00pm theater closes



Peter W. Staecker Ph.D.
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p.staecker@ieee.org

24 September 2013

Mazana Armstrong
IEEE Vancouver Section
Centennial Committee Chair
9812 Rathburn Drive
Burnaby, BC Canada V3J/7L1

Dear Mazana, and the Membership and Leadership of the IEEE Vancouver Section:

I cannot begin to share with you how deeply I regret not being able to join the IEEE Vancouver Section as it dedicates this extraordinary monument on the grounds of the Science World facility in Vancouver.

As one of only a few Sections that have already achieved a century of endeavor and achievement, the IEEE Vancouver Section already stands apart from its peers. The addition of this singular monument to the Vancouver cityscape is truly one of the singular accomplishments I have seen—by any Section—in my more than four decades as a member of IEEE.

I congratulate you on this remarkable feat, and commend the dedication of the many persons involved in bringing this incredible project to fruition. Though I am unable to attend this dedication, please know that my thoughts—and pride in your efforts—are with you on this truly memorable day.

Sincerely,

A handwritten signature in black ink that reads 'Peter Staecker'. The signature is fluid and cursive, with the first name 'Peter' being more prominent than the last name 'Staecker'.

Peter W. Staecker
2013 IEEE President and CEO