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- **Extreme CMOS manufacturability and reliability**
- **Trustworthy Smart-Grid infrastructures**



Stefan Ritt  
Paul Scherrer Institute

**Distinguished Lecturer**

Monday 15 July  
4:00 PM

TRIUMF Auditorium  
4004 Wesbrook Mall UBC

**Information**  
Jt Applied Physics chair  
Ahmed Hussein  
[Ahmed.Hussein@unbc.ca](mailto:Ahmed.Hussein@unbc.ca)

## Know your signals: waveform digitizing in the giga-sample range with switched capacitor arrays

Fast waveform digitizing is traditionally done with analog-to-digital converters (ADCs). These devices however hit their limits in resolution and power consumption when it comes to sampling rates far beyond the Giga-sample per second range (GSPS). An alternative for non-periodic signals are Switched Capacitor Arrays (SCA) that store an analog waveform in a series of capacitors, which are then digitized after a trigger at much lower speed.

While these chips have been used for two decades in particle physics, the recent improvements in CMOS technology allows for designs with resolutions of 12 bits, sampling speeds beyond 10 GSPS and power consumptions of a few tens of mW per channel. Putting many channels on a single chip makes it

possible to build data acquisition systems with several thousand channels at reasonable costs, space and power requirements. Obtaining the waveforms of particle detectors at high resolution allows excellent timing measurements down to a few pico-seconds, doing particle discrimination and efficient pile-up rejection.

This Talk covers the basic principles of SCAs, gives an overview of currently available chips and introduces advanced waveform processing techniques used in particle physics and gamma-ray astronomy. Experiences from the MEG experiment with 3000 SCA channels are reported. It finishes with an outlook for new chips currently under design and how they can be used in future experiments.

[https://meetings.vtools.ieee.org/meeting\\_view/list\\_meeting/18965](https://meetings.vtools.ieee.org/meeting_view/list_meeting/18965)



IEEE ULTRASONICS, FERROELECTRICS,  
AND FREQUENCY CONTROL SOCIETY





Vinod Prasad  
NTU Singapore

Monday 24 June  
5:30 pm to 7:00 pm

Room 2020, Kaiser Bldg  
2332 Main Mall, UBC

## Low complexity, reconfigurable digital filters and filter banks for channelization and spectrum sensing in multi-standard wireless communication receivers

Software defined radio (SDR) has been proposed as the solution to seamlessly support the existing and upcoming wireless communication standards. The fundamental idea of SDR is to replace the conventional analog signal processing in radio receivers with digital signal processing thus enabling the support of multiple communication standards by reconfiguration of the same hardware platform. SDR based cognitive radios (CRs) have the ability to sense the current spectrum utilization and change their behavioral and transmission characteristics dynamically so as to achieve efficient spectrum access. An important function in CRs is spectrum sensing, wherein the presence and (or) absence of channels of licensed users is to be detected in the wideband input signal in order to allow opportunistic access of the vacant frequency bands to the unlicensed users. In filter bank (FB) based spectrum sensing, the wideband input frequency range is split into uniform or non-uniform subbands using FBs and the presence of signals is then detected using techniques such as energy detection.

The channelizer, which consists of channel filters and FBs, is the most computationally intensive part of the SDR and CR based wireless communication receivers. In a typical CR, multiple radio channels corresponding to different wireless communication standards simultaneously coexist in the wideband input signal. These channels need to be accurately detected by the spectrum sensing block and then individually extracted by the channelizer, thus necessitating the ability to perform multi-standard channelization. Due to stringent area, power and cost specifications, channel filters and FBs that have low hardware resource utilization, low power consumption and high flexibility are desired for SDR and CR based wireless communication receivers.

**Speaker:** Vinod Prasad received his B. Tech. degree from University of Calicut, India in 1993 and the M. Engg and Ph.D. degrees from School of Computer Engineering, Nanyang Technological University, Singapore in 2000 and 2004 respectively. He has spent the first 5 years of his career in industry as an automation engineer at Kirloskar (India), Tata Honeywell (India), and Shell (Singapore). He joined the School of Computer Engineering at Nanyang Technological University (NTU), Singapore, in 2002, where he is currently an Associate Professor. [www.ntu.edu.sg/home/asvinod](http://www.ntu.edu.sg/home/asvinod)

Vinod's research interests include digital signal processing (DSP), low power and reconfigurable DSP circuits, software defined radio, cognitive radio and brain-computer interface. He has secured research grants from Ministry of Education (Singapore), Ministry of Defense (Singapore), DSO National Labs, European Aeronautic Defence & Space Company (EADS) Singapore, Embassy of France in Singapore, UK High commission (Singapore) and Singapore Millennium Foundation (SMF), amounting over S\$1.5 million as principal investigator. He has published about 160 research papers in refereed international journals and conferences. Currently, Vinod is leading a research team of 2 Postdoctoral Research Fellows and 7 PhD Students in Centre for High Performance Embedded Systems (CHiPES), NTU. He is a Senior Member of IEEE, Associate Editor of Circuits, Systems, and Signal Processing Journal (Springer), and an Editor of International Journal of Advancements in Computing Technology (IJACT). He has won the Nanyang Award for Excellence in Teaching in 2009, the highest recognition conferred by the University to individual faculty for teaching excellence.

**Cosponsor:** IEEE Circuits and Systems Society joint Chapter of the Vancouver/Victoria Sections

Light refreshments will be served. The event is open to public. We would greatly appreciate if you would please register so that we may more accurately estimate the room size and refreshments.

Registration: [https://meetings.vtools.ieee.org/meeting\\_registration/register/19115](https://meetings.vtools.ieee.org/meeting_registration/register/19115)

### Information

Solid-state Circuits chair  
Shahriar Mirabbasi  
[shahriar@ece.ubc.ca](mailto:shahriar@ece.ubc.ca)



IEEE COMPONENTS, PACKAGING, AND  
MANUFACTURING TECHNOLOGY SOCIETY





Jafar Savoj  
Xilinx

## Design of high-speed wireline transceivers for backplane communications in 28nm CMOS

This presentation describes the design of the architecture and circuit blocks for backplane communication transceivers. A channel study investigates the major challenges in the design of high-speed reconfigurable transceivers. Architectural solutions resolving channel-induced signal distortions are proposed and their effectiveness on various channels is investigated. Subsequently, the presentation describes the design of two fully-adaptive backplane transceivers embedded in state-of-the-art low-leakage 28nm CMOS FPGAs operating up to 12.5Gb/s and 13.1Gb/s. The two transceivers achieve BER < 10<sup>-15</sup> over a 33dB-loss backplane at 12.5Gb/s, and over a 31dB-loss backplane at 13.1Gb/s.

**Speaker:** Jafar Savoj received the B.Sc. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1996, and the M.Sc. and Ph.D. degrees in electrical engineering from the University of California, Los Angeles, in 1998 and 2001, respectively.

Dr. Savoj's areas of expertise include technology and product development for wireless, wireline, and analog systems. He is currently an Engineering Director with the Serdes Technology Group at Xilinx, San Jose, CA, and leads high-speed, low-power wireline transceiver development for FPGA applications. From 2008 to 2010, he was with Qualcomm, Santa Clara, CA, and led the advanced technology development

group for wireless connectivity. He was responsible for development of WLAN and Near Field Communication (NFC) transceivers, and low power chip-to-chip interfaces for mobile platforms. From 2005 to 2008, he was a principal engineer at Rambus, where he developed ultra-high-speed data converters for software programmable wireline transceivers. Prior to that, he held design engineering positions at Marvell Semiconductor, Santa Clara, CA, focusing on fiber channel and Gigabit Ethernet transceivers; and at Transpectrum, Los Angeles, CA, architecting 10-Gb/s and 40-Gb/s optical transceivers in CMOS technology. He held a lecturing position at Stanford University in 2004. He is the author of High-Speed CMOS Circuits for Optical Receivers (Kluwer, 2001).

Dr. Savoj was a recipient of the IEEE Solid-State Circuits Society Predoctoral Fellowship for 2000–2001, and the Beatrice Winner Award for Editorial Excellence at the 2001 ISSCC, and the Design Contest Award of the 2001 Design Automation Conference. He serves as a technical program committee member of ISSCC (Analog Subcommittee). He served as a technical program committee member of the IEEE Custom Integrated Circuits Conference (CICC) from 2001 to 2007 and the IEEE Symposium on VLSI Circuits from 2007 to 2011. He was an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 2008 to 2011 and a Guest Editor for the Journal in 2005, 2006 and 2011.

### Distinguished Lecturer

Thursday 04 July  
5:30 pm to 7:00 pm

Room 2020, Kaiser Bldg  
2332 Main Mall, UBC

Light refreshments  
will be served.

The event is open to  
public

### Information

Solid-state Circuits chair  
Shahriar Mirabbasi  
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## International Professional Communication Conference

July 15 – 17, 2013  
University of British Columbia

**Register Today! Register by July 13  
and save \$50 on registration costs.**

<http://pcs.ieee.org/ipcc2013/>

The annual International Professional Communication Conference sponsored by the IEEE Professional Communication Society. Attended by professionals from around the world, the International Professional Communication Conference (IPCC) offers an opportunity for colleagues and experts to meet and learn about leading-edge developments in communication theory and technology. Attendees include technical and professional communicators, practicing



**Register by July 13 and save \$50  
on IPCC 2013 registration costs!**

engineers, and educators and students in engineering communication. This year's theme explores the complex intersection of rapidly emerging technologies and ever-changing linguistic, social, national, and cultural borders in today's increasingly globalized world.





Ahmed Hussein  
University of Northern BC

Monday 24 June  
4:00 PM

## Dual Fluid Reactor, a new concept of a fast nuclear reactor

The Dual Fluid Reactor (DFR) is a novel nuclear reactor concept based on the Generation IV Molten-Salt Reactor (MSR) concept and the liquid-metal cooled reactors (SFR, LFR) with the major improvement that the molten-salt fuel is not used as coolant but the heat is removed in a separate liquid-lead loop. It is a fast reactor, that consumes all fissionable materials like U233, U235, U238, Pu239, natural Thorium, etc.

It has much simpler design, passive safety, and produces much less nuclear waste than currently used nuclear power reactors. It does not emit any radioactivity or green house gases during operation. It costs as much as a coal fed power station to construct and operate.

There are more benefits that will be discussed in the talk.

TRIUMF Auditorium  
4004 Wesbrook Mall UBC



IEEE ULTRASONICS, FERROELECTRICS,  
AND FREQUENCY CONTROL SOCIETY

### Information

Joint Applied Physics  
chair

Ahmed Hussein

Ahmed.Hussein@unbc.ca

## 2013 IEEE POWER & ENERGY SOCIETY GENERAL MEETING

SHAPING THE FUTURE ENERGY INDUSTRY

Vancouver, British Columbia, Canada July 21-25 2013

This largest IEEE PES annual conference attracts professionals from every segment of the electric energy industry. It features a comprehensive technical program, including Super Sessions, panel sessions, technical committee meetings and standards activities. Not to be missed are the technical tours, a student program, companion activities and more. This year's theme is Shaping the Future Energy Industry. For more information about the conference, please visit the conference website at <http://www.pes-gm.org/2013>.

The early bird registration deadline is less than a month away. I invite you to register for the conference and, in addition to the regular technical program, also attend various optional events which are selling out fast, for example technical tours and tutorials. Based on the statistics so far, we are anticipating what may be the largest IEEE PES General Meeting to date. I hope you can join us and make this an event to remember.

We are also in need of many volunteers for the conference, so if you reside in Lower Mainland and you would like to learn how you can volunteer and attend the conference for free, more information is available here. For those of you living outside the Lower Mainland, we have just added another block of hotel rooms at the preferred conference rate, please check the conference website for information how to book your hotel room.

If you have any questions about the conference or how you can get involved, please send me an email. I look forward to seeing you at the General Meeting!

Mazana Armstrong Chair

IEEE PES General Meeting 2013 Vancouver

[pesgm2013-vancouver@ieee.org](mailto:pesgm2013-vancouver@ieee.org) [www.pes-gm.org/2013/](http://www.pes-gm.org/2013/)



Vinod Prasad  
NTU Singapore

Tuesday 25 June  
2:00 pm to 3:30 pm

ASB 10900 (IRMACS  
Presentation Studio)  
SFU, Burnaby

## Efficient signal processing techniques towards the development of EEG based Brain-Computer Interface (BCI)

Brain-Computer Interface (BCI) is an emerging technology that enables human brain to communicate with external world solely by brain signals, bypassing its normal output pathway of nerves and muscles. Capability of BCI for controlling external applications such as computer screen, wheel chair, robotic arm, neuroprosthetic devices etc. makes it a promising communication tool for paralyzed patients. Neural features in Electroencephalogram (EEG) related to the mental imagination of motor movement, termed motor imagery (MI), are potential candidates for developing EEG-based BCI. Activations in brain's motor cortex during MI result in distinct EEG patterns. BCI performance is strongly correlated to accurate identification of the relevant features.

This talk will present some of the efficient algorithms which we proposed towards the development of MI-based BCI. A major challenge in any MI based BCI is the variability of MI patterns in temporal, spectral and spatial domains across different subjects over time. Our Discriminative Filterbank Common Spatial Pattern (DFBCSP) addresses the inter-subject variability of MI patterns by effectively estimating the subject-specific informative frequency bands for differentiating various MI tasks. Another new adaptive approach named as Adaptively Weighted Spectral Spatial Patterns (AWSSP) tracks the variability of the informative bands over time by adaptively computing the discriminative capability of various frequency components. Proposed methods offer higher BCI performance in terms of classification accuracy compared to the state-of-art method. We have also proposed robust algorithms for classifying and decoding voluntary hand movement execution parameters such as direction and speed. The proposed Wavelet CSP (W-CSP) algorithm extracts low frequency components of EEG that encodes movement parameter information. Our Multiple Linear Regressor models can reconstruct the movement speed profile from W-CSP filtered EEG. The talk will also present preliminary results of our work to

understand the effect of neurofeedback games on the cognitive skills of healthy subjects with the intention of developing serious games for treating attention-deficit children.

**Speaker:** Vinod Prasad received his B. Tech. degree from University of Calicut, India in 1993 and the M. Engg and Ph.D. degrees from School of Computer Engineering, Nanyang Technological University, Singapore in 2000 and 2004 respectively. He has spent the first 5 years of his career in industry as an automation engineer at Kirloskar (India), Tata Honeywell (India), and Shell (Singapore). He joined the School of Computer Engineering at Nanyang Technological University (NTU), Singapore, in 2002, where he is currently an Associate Professor. [www.ntu.edu.sg/home/asvinod](http://www.ntu.edu.sg/home/asvinod)

Vinod's research interests include digital signal processing (DSP), low power and reconfigurable DSP circuits, software defined radio, cognitive radio and brain-computer interface. He has secured research grants from Ministry of Education (Singapore), Ministry of Defense (Singapore), DSO National Labs, European Aeronautic Defence & Space Company (EADS) Singapore, Embassy of France in Singapore, UK High commission (Singapore) and Singapore Millennium Foundation (SMF), amounting over S\$1.5 million as principal investigator. He has published about 160 research papers in refereed international journals and conferences. Currently, Vinod is leading a research team of 2 Postdoctoral Research Fellows and 7 PhD Students in Centre for High Performance Embedded Systems (CHiPES), NTU. He is a Senior Member of IEEE, Associate Editor of Circuits, Systems, and Signal Processing Journal (Springer), and an Editor of International Journal of Advancements in Computing Technology (IJACT). He has won the Nanyang Award for Excellence in Teaching in 2009, the highest recognition conferred by the University to individual faculty for teaching excellence.

Light refreshments will be served. The event is open to public. We would greatly appreciate if you would please register so that we may more accurately estimate the room size and refreshments.

Registration: [https://meetings.vtools.ieee.org/meeting\\_registration/register/19111](https://meetings.vtools.ieee.org/meeting_registration/register/19111)

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# Technical field trip to Victoria

**Friday 12 July 8AM till 8PM**

We will catch the 9AM ferry at the Tsawwassen terminal.  
Our tour in Victoria will finish around 5PM, and we will catch the 6PM ferry back to Vancouver.

The IEEE Engineering in Medicine and Biology (EMB) Vancouver chapter and UBC Biomedical Engineering Graduate Association (BMEGA) club are organizing a technical field trip to Victoria. This field trip will include

- Tour of StarFish Medical (<http://starfishmedical.com>)
- Tour of CanAssist (<http://canassist.ca>)
- Presentation of local industries at University of Victoria (UVic) (<http://www.engr.uvic.ca/~willerth/>)

This is an excellent opportunity to visit one of the leading biomedical companies in BC, and to find out about job opportunities offered in Victoria. You will be able to network.

## Agenda

9:00AM till 11:30AM Transit from Tsawwassen to StarFish Medical

11:30AM – 12:30PM

StarFish tour by Scott Phillips, president of StarFish

12:30PM – 1:30PM

StarFish presentation with light food and snack, followed by networking event

1:30PM – 2PM

Transit from StarFish to UVic

2PM – 3PM

CanAssist tour by Michael Shannon, director of CanAssist

3PM – 5PM

Tour of Willerth Laboratory and presentation of local industries by Dr. Willerth

5PM – 7:30PM

Transit from StarFish to Vancouver

## Cost:

This trip is partially subsidized by IEEE EMB and BMEGA for the students. The fee will include all transportation costs and light lunch.

For students: \$25 (includes all transportation costs and light lunch)

For professionals: \$45 (includes all transportation costs and light lunch)

## Registration

Space is limited with priorities given to IEEE EMB and BMEGA members. To register, please send an email to Sara ([sarak@ieee.org](mailto:sarak@ieee.org)) or Kousha ([kousha.talebain@gmail.com](mailto:kousha.talebain@gmail.com)). We will create an invoice and forward it to you; You can then pay through PayPal using your PayPal account or credit card. Please indicate if you are a student or a professional. Please include your school name and student ID if applicable. You will receive a more detailed itinerary closer to the date of event.

## About StarFish Medical

Today, StarFish is a leading service provider in the medical device industry. They have successfully partnered with many innovative companies to create breakthrough products for numerous medical specialty areas. They have won numerous awards including:

- 2010 I.D. Magazine Annual Design Review Honorable Mention. StarFish was recognized by I.D. for their outstanding work on the VisionAid AMD treatment system.

- 2010 Red Dot Award Honorable Mention

StarFish received an honorable mention in the prestigious Red Dot awards for innovative design of a medical product with the OsseoPulse™ bone regeneration system.

- 2010 Nomination for Ernst & Young Entrepreneur of the Year  
Phillips was nominated in the Life Sciences category for British Columbia.

For more information, please visit <http://starfishmedical.com>

## About CanAssist

CanAssist is an organization at the University of Victoria that is dedicated both to helping those with disabilities improve their quality of life and to increasing awareness and knowledge of disability issues. "We are primarily a service-based organization, but employ the considerable educational and research resources available to us at UVic. We focus on developing practical, customized technologies for people with disabilities, as well as providing innovative programs where there is a gap in existing services."

## About Willerth Laboratory

"The Willerth lab uses quantitative approaches to significant biological problems in the areas of tissue engineering and regenerative medicine. One of the main areas of research focuses on the development of bioactive scaffolds for directing stem cell differentiation. Specifically, our lab studies the behavior of embryonic stem cells and induced pluripotent stem cells inside of biomaterial scaffolds as a method for engineering tissues. In particular, we are interested in using induced pluripotent stem cells as an exciting alternative to the use of traditional embryonic stem cell lines. IPS cells are generated from adult somatic cells, such as skin cells, by up regulating the expression of specific factors that restore the ability of the cells to differentiate into any type of cell."



**IEEE Engineering in  
Medicine and Biology**

Engineering in Medicine  
& Biology chair  
Rob Rohling  
[rohlink@ece.ubc.ca](mailto:rohlink@ece.ubc.ca)





# SHAPING THE FUTURE ENERGY INDUSTRY

**2013 IEEE PES General Meeting  
Vancouver, BC | July 21-25**

**The 2013 IEEE Power & Energy Society General Meeting is being held at the Vancouver Convention Centre, British Columbia, Canada.**

The PES General Meeting attracts thousands of professionals from every segment of the electric power and energy industry. It features a comprehensive technical program, including Super Sessions, panel sessions, tutorials, technical committee meetings and standards activities, PLUS excellent technical tours, a student program, companion activities and much more. This year's theme is **Shaping the Future Energy Industry.**

**Super Sessions for the 2013 program include:**

- Electricity Supply to Rural and Remote Communities
- Transmission System Efficiency and Reliability Improvements
- Impacts of Geomagnetic Disturbance (GMD) Events on Electric Power Systems
- Innovation and Advancements in Protection, Automation and Control for Evolving Power Systems
- Generation Mix Strategies: Solving Energy Production Challenges of the 21st Century

*This year, the PES General Meeting takes place in Vancouver, BC. Majestic mountains, sparkling ocean, rainforests and beautiful foliage all four seasons make Vancouver one of the most beautiful cities in the world - and a wonderful place to visit in July! Reserve your room at the Vancouver Marriott Pinnacle Downtown Hotel or the Renaissance Vancouver Harbourside Hotel.*

**REGISTER NOW**

**For more information and program  
updates visit: [pes-gm.org/2013](http://pes-gm.org/2013)**



# Play golf today and improve tomorrow

## IEEE PES Scholarship Plus Initiative golf outing

### Sunday 21 July

### Furry Creek Golf Course

Registrations are now being taken for the IEEE PES Scholarship Plus Initiative Program Golf Outing scheduled for July 21, 2013 at Furry Creek Golf Course in Furry Creek, BC. The golf outing is being sponsored by the IEEE Power & Energy Society and is being held prior to the 2013 IEEE PES General Meeting. If you participate in this golf outing, you will enjoy a great day of camaraderie and friendly competition between golfing friends and colleagues who will tee it up all for the benefit of the IEEE PES Scholarship Plus Initiative and the Next Generation of Power and Energy Engineers. This golf outing will benefit the expansion of the IEEE PES Scholarship Plus Initiative Program to Canada.

Furry Creek is not a course that one merely plays - it is an enriching adventure to be savored. Considered one of the most beautifully landscaped playgrounds in British Columbia, Furry Creek delivers an unforgettable experience with its breathtaking beauty, dramatic play and first-class facilities. As BC's most scenic golf course, Furry Creek perfectly captures the most spectacular qualities of this part of the country. This par 72, 18-hole golf course designed by Robert Muir Graves and built in 1993 offers panoramic ocean views and encounters with abundant wildlife, and is just 35 minutes north of Vancouver, along the scenic Sea to Sky Highway to Whistler.

The cost to participate in the golf outing is US\$175 per person. Sponsorship opportunities are also available. There are a limited number of seats available for this golf outing that will offer all competitors the opportunity to win individual and team prizes. Early registration is encouraged as tee times will be sold on a first-come, first-served basis. The day's outing begins at 9:00 a.m. with a shotgun start followed by awards presentations. Visit the registration page and make your reservation.

The IEEE PES Scholarship Plus Initiative provides multi-year scholarships to qualifying U.S. and Canadian electrical engineering undergraduate students. Scholars receive up to three years (US\$7,000) of funding interspersed with up to two years of valuable, hands-on career experience. The program, made possible by donations to the IEEE Power & Energy Society Scholarship Fund of the IEEE Foundation, is in its 3rd year. Since its inception, the program has supported a total of 265 scholars attending 109 universities, including Ivy League colleges, flagship state universities and prestigious engineering colleges across the US. The 2013 program goal is to distribute more than 400 scholarships in the US & Canada. If you have any questions, please send us an email

## IEEE PES Scholarship Plus Initiative has been expanded to Canada

### *Applications are being accepted*

Over the past two years, the IEEE Power & Energy Society has distributed over US\$642,000 in scholarships to 265 students from 109 universities within the United States. In 2013, we are expanding the IEEE PES Scholarship Plus Initiative to include students in Canada. Our goal this year is to distribute more than 400 scholarships to electrical engineering students in the USA and Canada!

The PES Scholarship Plus Initiative™ is a scholarship and career experience program that was created in response to the looming workforce shortfall in the power and energy industry. Our goal is simple: increase the number of well-qualified, entry-level engineers by helping students. PES Scholarship Details We are offering up to US\$7,000 and assistance with career experience opportunities to qualifying students!

You must be a full-time student working towards a bachelor's degree in electrical engineering, a US or Canadian citizen or permanent resident of either country, willing to take power engineering courses and have a GPA of at least 3.0. Engineering students early in their

college careers are encouraged to apply, even if in June 2013 they have not yet declared electrical engineering as their major.

In Fall 2013, the individual must be enrolled in an electrical engineering program working toward a bachelor's degree. Here's how it works: ? Eligible students should apply online by June 30th, 2013 at <http://www.eescholarship.org/application> ? Recipients will be selected by PES volunteers with industry and academic backgrounds. In the fall, recipients will be notified of their selection and be provided with information on how to arrange for a career experience with industry-leading companies. ? The scholarship funds will be distributed to your university/college for deposit and credit against your student account. Don't delay, click below to start your scholarship application or follow us on Facebook. Apply Now <http://www.ee-scholarship.org/application> Visit Us on Facebook <http://www.facebook.com/ieeepes.scholarship.plus>

If you have any questions, please contact Dan Toland, IEEE PES Scholarship Plus Initiative ([pessscholarship-info@ieee.org](mailto:pessscholarship-info@ieee.org))



## ***Welcome.. recent arrivals to IEEE Vancouver!!***

Fatemeh Aezinia .....	GS	Mai Hassan .....	GS	Thanh Son Pham .....	M
Hafiz Munsub Ali .....	GS	Simon Hecker .....	ST	Oldooz Pooyanfar .....	ST
Babak Assadsangabi .....	GS	Taylor Hetherington .....	GS	Shokoofeh Pourmehr .....	GS
Thomas Au .....	GS	Mark Hiebert .....	M	Ming Qi .....	M
Bryce Baxter .....	M	Sabine Hindermann .....	ST	Danica Reardon .....	ST
Graeme Bernier .....	ST	Brian Hofer .....	ST	Matthew Reid .....	M
Max Bethune-Waddell .....	ST	Tejpaul Hoonjan .....	ST	Cory Reid .....	M
Fatemeh Aezinia .....	GS	Mike Hsiao .....	ST	Thomas Ries .....	M
Hafiz Munsub Ali .....	GS	Jinzhong Hua .....	M	Kevin Russell .....	ST
Babak Assadsangabi .....	GS	Hao Yu Huang .....	ST	Janine Cindy Santiago .....	ST
Thomas Au .....	GS	Yingwei Huang .....	GS	Marinko Sarunic .....	M
Bryce Baxter .....	M	Helen Iosfin .....	M	Daniel Schwanke .....	M
Graeme Bernier .....	ST	Barry Ivison .....	M	Nimesh Shah .....	M
Max Bethune-Waddell .....	ST	Pooya Jaferian .....	GS	Stan Shear .....	M
Chongyuan Bi .....	GS	Brian Just .....	M	Ahmed Sherwali .....	GS
Justin Blackman .....	ST	Wasim Kapadia .....	ST	Won-Chul Shin .....	M
Dieter Blum .....	M	Jeremy Kawahara .....	GS	Wilson Shiu .....	GS
Colin Brown .....	GS	Amir Kenarsari Anhari .....	GS	Douglas Sim .....	GS
Jennifer Busler .....	M	Sayed Hossein Khatoonabadi .....	GS	Krishneil Singh .....	ST
Ritesh Chand .....	ST	Danil Khomenko .....	ST	Jason Smith .....	M
Li Chen .....	AM	Emanuel Koseos .....	ST	Yilun Song .....	ST
Zheng Chen .....	GS	Gunes Kucukyilmaz .....	ST	Tom Stefanski .....	M
Ying Chen .....	GS	Roshan Kumar .....	ST	Philip Stoyanov .....	ST
Fei Chen .....	GS	Choong-Hoon Kwak .....	GS	Eric Swanlund .....	ST
Yiwu Chen .....	ST	Daniel Lang .....	ST	Alex Tam .....	ST
William Cheung .....	M	Timothy Lee .....	ST	Arash Tavighi .....	GS
Michael Chiang .....	ST	SeungJun Lee .....	ST	Emmanuel Rossignol Thepie Fapi .....	M
Paul Christensen .....	M	WenHui Li .....	ST	Alan Thompson .....	M
Savio Chu .....	M	Jianqiao Li .....	GS	Michael Todorovic .....	ST
Jonny Chung .....	ST	Ang Li .....	GS	Hamid Reza Tohidypour .....	GS
Christopher Collier .....	GS	Cyprian Libera .....	M	Samer Toukan .....	M
Trevor Condon .....	ST	Ye Lin .....	ST	Daniel Troniak .....	GS
Michael Conroy .....	M	David Lin .....	M	Chin-Tsai Tsai .....	ST
Carlo Cossette .....	ST	Geoff Littler .....	M	Frederic Tschanz .....	M
Mark Crapper .....	ST	Mofei Liu .....	GS	Chao Tsan Tseng .....	ST
Foad Davani .....	M	Charlie Liu .....	ST	Michael Tsirolnikov .....	M
Francisco De Alba .....	GS	Ana Lopez Fernandez .....	ST	Jason Tu .....	GS
Danny deSousa .....	M	Jessica Ma .....	ST	Frederick Tung .....	GS
Paramjit Dhesi .....	ST	Bojiang Ma .....	GS	Sergey Uchaikin .....	M
Navdeep Dhillon .....	ST	Farid Mabrouk .....	GS	Carlos Uribe Munoz .....	GS
Weiguang Ding .....	GS	Tibor Magyarosi .....	M	Oscar van der Meer .....	M
Han Du .....	ST	Andrew Mahoney .....	M	Jacobus Van Eeden .....	ST
Suyang Duan .....	GS	Vincent Mantle .....	M	Tristan van Leeuwen .....	M
Sarah Elmasry .....	ST	Julieta Martinez .....	GS	Alexander Viel .....	M
H D Kenneth Epp .....	M	Amir Hossein Masnadi Shirazi Neja .....	GS	guihua Wang .....	M
Mona Erfani Joorabchi .....	GS	Victor Mateescu .....	GS	Xing Wang .....	GS
Fatemeh Eslami .....	GS	Michael McIvor .....	M	Scott Warren .....	M
Mario Estevez .....	ST	Trent McKeen .....	M	Shibo Weng .....	ST
Mustafa Fanaswala .....	GS	Darren McRae .....	M	Derek White .....	M
Mark Farrow .....	ST	Ahmed Medhioub .....	ST	Alex Wiecke .....	ST
Dusanka Firaunovic .....	M	Reyad Mehruz .....	GS	Jess Wilson .....	M
Brian Fisher .....	M	Omid Mohareri .....	GS	Ben Wong .....	ST
Gordon Frank .....	M	Valiallah Monajjemi .....	GS	Patrick Wong .....	ST
Alexandre Frechette .....	GS	Soudeh Mousavi .....	ST	Di Wu .....	ST
Wilson Wai Lun Fung .....	GS	Andrew Ngai .....	ST	Xiaoye Xia .....	M
Lu Gan .....	ST	Andy Ngauv .....	ST	Tingting Xu .....	GS
Red Kernel Garsuta .....	ST	Bowen Nie .....	ST	Shin-Hann Yang .....	ST
Erol Girt .....	M	Brian Page .....	M	Xi Yue .....	GS
Ashleigh Gonzales .....	GS	Andrew Parker .....	M	Sajjad Zadkhast .....	GS
Emma Gosselin .....	ST	Graham Percival .....	GS	Benxin Zhang .....	GS
Micheal Griffin .....	ST	Christian Petersen .....	M	Cyrus Zhang .....	ST
Grahame Hamilton .....	M	Kalyani Phadke .....	M	David Zlotnik .....	GS
Brandon Hart .....	ST				

AF Affiliate - AM Associate Member - F Fellow - GS Graduate Student Member - LF Life Fellow  
LM Life Member - LS Life Senior - M Member - SM Senior Member - ST Student Member



Abdallah Shami  
U. Western Ontario

Wednesday 10 July  
2:30 pm to 3:30 pm

Room ASB 9705  
Simon Fraser University

#### Cosponsor

IEEE Circuits and  
Systems Society  
Victoria Sections

#### Information

Circuits and Systems  
chair Ljiljana Trajkovic  
ljilja@cs.sfu.ca

ED 01JULY13

## Multihoming: scheduling, modelling, and congestion window management

Known as multihoming, devices with more than one network interface can enhance their performance capabilities by harnessing unused resources from alternative access networks. Whether it is improved reliability or sheer throughput potential, network devices will benefit from a multihomed framework. Unfortunately, our current means of guaranteeing reliability while maintaining quality control, specifically, the transmission control protocol (TCP), does not support multihoming. Despite the latter, a relatively young transport layer standard called the stream control transmission protocol (SCTP), incorporates multihoming into its design. In this talk, we present the state-of-the-art multihoming techniques using SCTP. A comprehensive overview of three main research areas will be presented, namely: handover management, concurrent multipath transfer (CMT), and congestion window management.

**Speaker:** Abdallah Shami received the B.E. degree in Electrical and Computer Engineering from the Lebanese University, Beirut, Lebanon in 1997, and the Ph.D. Degree in Electrical Engineering from the Graduate School and University Center, City University of New York, New York, NY in September 2002. In September 2002, he joined the Department of Electrical Engineering at Lakehead University, Thunder Bay, ON, Canada as an Assistant Professor. Since July 2004, he has been with Western University, Canada where he is currently an Associate Professor in the Department of Electrical and Computer Engineering. His current research interests are in the area of wireless/optical networking. Dr. Shami is currently an Associate Editor for IEEE Communications Letters and IEEE Communications Tutorials and Survey. Dr. Shami has chaired key symposia for IEEE GLOBECOM, IEEE ICC, IEEE ICNC, and ICCIT. Dr. Shami is a Senior Member of IEEE



Saman Zonouz  
University of Miami

Thursday 25 July  
3:30 p.m

Kaiser 2020  
2332 Main Mall  
UBC

## Trustworthy Smart-Grid infrastructures: threats, challenges, and countermeasures

Secure and reliable operation of next-generation cyber-physical systems, specifically power grid infrastructures, will require effective trusted computing bases to provide situational awareness, security property verification, and intrusion tolerance capabilities. Continuous and precise comprehension of the system's security status and potential threats will enable operators and/or automated response systems to prepare proactively against adversarial coordinated activities, such as coordinated cyber and physical intrusions.

**Speaker:** Saman Zonouz is an Assistant Professor in the Electrical and Computer Engineering Department at the University of Miami since August 2011, and the Director of the 4N6 Cyber Security and Forensics Laboratory. He has been awarded the Faculty Fellowship Award by the Air Force Office of Scientific Research in 2013, UM Provost Research award in 2011, as well as EARLY CAREER Research award from the University of Miami in 2012. His group's research projects have been funded by NSF, ONR, DOE/ARPA-E, and Fortinet Corporation.

In this talk, we will overview the power grid security problem, and in particular, potential threats and possible countermeasures in such cyber-physical environments. Additionally, we will review several solutions to model, detect, and tolerate complex security incidents in computing, physical, or communication assets of the power grid in a real-time manner.

His current research focuses on Systems Security and Privacy, Intrusion Detection, Forensics, and Response, as well as Trustworthy Critical Cyber-Physical Power-Grid Infrastructures. He obtained his Ph.D. in Computer Science, specifically, Intrusion Tolerance Solutions for the Power-Grid, from University of Illinois at Urbana-Champaign (UIUC) in 2011.



**Information**  
Computer Society chair  
Sathish Gopalakrishnan  
sathish@ece.ubc.ca

ED 22JULY13



Alexander Apostolov  
OMICRON Electronics

Friday 12 July  
9.00 am – 4.30 pm

Centre Auditorium  
BC Hydro Edmonds  
6911 Southpoint Dr Bby

Light breakfast  
refreshment and  
lunch will be served

Registration fees  
IEEE student member  
CAD 25.00  
IEEE members  
CAD 40.00  
Non members  
CAD 75.00

#### Information

Jahangir Khan  
IAS Chair

[jahangir.khan@powertechlabs.com](mailto:jahangir.khan@powertechlabs.com)

Joint Power & Energy chair  
Rama Vinnakota  
[Rama.Vinnakota@bchydro.com](mailto:Rama.Vinnakota@bchydro.com)



ED 05JUL13

## Workshop: IEC 61850 fundamentals, applications and benefits

In the Smart Grid Roadmap IEC 61850 has been identified as one of the cornerstone technologies. This is a one day seminar that introduces the fundamental concepts of IEC 61850 and then focuses on the applications and benefits. The following topics will be presented.

1. Introduction of IEC 61850: This opening session will look at the history of the IEC 61850 standard, the current state of development, as well as the pros and cons of adopting this standard as a platform for substation automation systems.
2. IEC 61850 Systems and Their Components: Application of IEC 61850 devices and systems requires good understanding of the functional hierarchy and the components of the system. This lecture describes different possible implementations of IEC 61850 based systems and gives some examples of IEC 61850 based substations projects around the world.
3. Ethernet Communications in Substations: Ethernet is the underlying communications protocol in IEC 61850 based substation automation systems. The structure of Ethernet messages needs to be understood well in order to implement and troubleshoot such systems. Priority tagging and V-Lan are described as well.
4. GOOSE Messages: GOOSE messages are one of the key differentiators of IEC 61850 in comparison with other substation communication protocols. The structure of GOOSE messages, repetition mechanisms and Publishing/ Subscription concepts are discussed.
5. IEC 61850 Process Bus: Sampled Values Publishing and Subscription: Process bus is the foundation for the development of the substations of the twenty first century. The concept of process bus, implementation agreements, applications and benefits are presented.
6. Substation Configuration Language Based Engineering: The Substation Configuration Language (SCL) of IEC 61850 is one of the main tools that allow the shift to a different engineering process based on the different XML based files defined in the standard - ICD, CID, SCD. XML and the different SCL files and their use in relation to system testing are discussed.
7. IEC 61850 Testing - Equipment Requirements and Tools: IEC 61850 based substation automation and protection systems are different from conventional systems due to the use of communications to replace hard wiring for many functions in the substation. This imposes different requirements for the testing equipment and software tools that are described in the lecture.

8. Migration Strategies: IEC 61850 is designed for implementation in existing and new installations and supports the integration of IEDs designed specifically for optimal performance based on it, as well as to allow the integration of legacy IEDs and even electromechanical relays. Tools supporting different migration strategies are described together with possible migration scenarios and a look at the future of IEC 61850 based substation protection, automation and control systems.

**Speaker:** Dr. Alexander Apostolov received MS degree in Electrical Engineering, MS in Applied Mathematics and Ph.D. from the Technical University in Sofia, Bulgaria. He has worked for fourteen years in the Protection & Control Section of Energo project Research and Design Institute, Sofia, Bulgaria.

From 1990-94 he was Lead Engineer in the Protection Engineering Group, New York State Electric & Gas where he worked on the protection of the six-phase line, application of microprocessor relays, programmable logic and artificial intelligence in protection. 1994-95 he was Manager of Relay Applications Engineering at Rochester - Integrated Systems Division. 1995-96 he was Principal Engineer at Tasnet. 1996-2006 he was Principal Engineer for AREVA T&D Automation.

He is presently Principal Engineer for OMICRON electronics in Los Angeles, CA. He is IEEE Fellow and Member of the Power Systems Relaying Committee and Substations Subcommittee. He is the past Chairman of the Relay Communications Subcommittee, serves on multiple IEEE PES Working Groups and is Chairman of Working Group C9: Guide for Abnormal Frequency Load Shedding and Restoration.

He has been actively involved for more than 10 years in the development of UCA 2 and IEC 61850. He is member of IEC TC57 Working Groups 10, 17, 18. He is Chairman of the Technical Publications Subcommittee of the UCA International Users Group. He is member of CIGRE and works on CIGRE WG B5.07, B5.09 and B5.36. He is Convener of B5.27 Standard Protection Schemes.

He holds four patents and has authored and presented more than 300 technical papers. Dr. Apostolov is also the Editor-in-Chief of the PAC World magazine – the global forum of the protection, automation and control industry. He is also Adjunct Professor at the Department of Electrical Engineering, Cape Peninsula University of Technology, Cape Town, South Africa.

**Registration required - please visit:**

<http://tinyurl.com/kpro8ea> OR [https://meetings.vtools.ieee.org/meeting\\_registration/register/19119](https://meetings.vtools.ieee.org/meeting_registration/register/19119)





David Z. Pan  
University of Texas

**Distinguished Lecturer**

**FIRST EVENT**

Monday 15 July  
04:00PM to 05:30PM

Room 2020, Kaiser Bldg  
2332 Main Mall UBC

**Information**

Solid-state Circuits chair  
Shahriar Mirabbasi  
shahriar@ece.ubc.ca

**SECOND EVENT**

Monday 22 July  
01:30PM to 03:00PM

Room EOW 430  
U.Victoria, Victoria BC

**Information**

Circuits and Systems  
chair Ljiljana Trajkovic  
ljilja@cs.sfu.ca

## Design for manufacturability and reliability in extreme CMOS scaling and beyond

Design for Manufacturability and Reliability in Extreme CMOS Scaling and Beyond As the CMOS feature enters the era of extreme scaling (14nm, 11nm and beyond), the IC manufacturability/printability challenges are exacerbated. Meanwhile, the vertical scaling with 3D-IC integration using through-silicon vias (TSVs) has gained tremendous momentum and initial industry adoption, which can further extend the Moore's Law even the horizontal scaling stops ultimately. However, as TSV involves disruptive manufacturing technologies, new modeling and design techniques need to be developed for reliable 3D IC integration. This talk will first show how the nanolithography envelope is being pushed with novel design/process integration for multiple patterning lithography as well as other emerging technologies. In 3D-IC, TSV induced thermal/mechanical stress not only results in systematic performance variations, but also leads to mechanical and electrical reliability concerns. Cross-layer modeling and physical design techniques will be discussed to achieve reliable 3D-IC integration.

As the CMOS feature enters the era of extreme scaling (14nm, 11nm and beyond), the IC manufacturability/printability challenges are exacerbated. Meanwhile, the vertical scaling with 3D-IC integration using through-silicon vias (TSVs) has gained tremendous momentum and initial industry adoption, which can further extend the Moore's Law even the horizontal scaling stops ultimately. However, as TSV involves disruptive manufacturing technologies, new modeling and design techniques need to be developed for reliable 3D IC integration. This talk will first show how the nanolithography envelope is being pushed with novel design/process integration for multiple patterning lithography as well as other emerging technologies. In 3D-IC, TSV induced thermal/mechanical stress not only results in systematic performance variations, but also leads to mechanical and electrical reliability concerns. Cross-layer modeling and physical design techniques will be discussed to achieve reliable 3D-IC integration.

**Speaker:** David Z. Pan received his Ph.D. in computer science from UCLA in 2000. He was a Research Staff Member at IBM T. J. Watson Research Center from 2000 to 2003. Since 2003, he has been an Assistant/Associate/Full Professor with the Department of Electrical and Computer Engineering, UT Austin. He has published over 180 highly refereed journal and conference papers. He has served as an Associate Editor for IEEE Transactions on CAD, IEEE Transactions on VLSI, IEEE Transactions on CAS - I & II, IEEE CAS Society Newsletter, Science China Information Sciences, Journal of Computer Science and Technology. He has served as Chair of the IEEE CAS/CEDA CANDE Technical Committee and the ACM/SIGDA Physical Design Technical Committee, Program/General Chair of ISPD, TPC Subcommittee Chair for DAC, ICCAD, ASPDAC, ISLPED, ICCD, ISCAS, and so on. He is a working group member of the International Technology Roadmap for Semiconductor (ITRS). He serves in the ACM/IEEE Design Automation Conference (DAC 2014) Executive Committee.

He has received a number of awards, including DAC Top 10 Author in Fifth Decade, DAC Prolific Author Award, 9 Best Paper Awards (ASPAC 2012, ISPD 2011, IBM Research 2010 Pat Goldberg Memorial Best Paper Award in CS/EE/Math, ASPAC 2010, DATE 2009, ICICDT 2009, SRC Techcon in 1998, 2007 and 2012), Communications of the ACM Research Highlights (2013), ACM/SIGDA Outstanding New Faculty Award (2005), NSF CAREER Award (2007), SRC Inventor Recognition Award three times, IBM Faculty Award four times, UCLA Engineering Distinguished Young Alumnus Award (2009), ISPD Routing Contest Awards (2007), eASIC Placement Contest Grand Prize (2009), ICCAD'12 CAD Contest Award, among others. He was an IEEE CAS Society Distinguished Lecturer for 2008-2009.

**REGISTRATION**

15 July event - [https://meetings.vtools.ieee.org/meeting\\_view/list\\_meeting/19315](https://meetings.vtools.ieee.org/meeting_view/list_meeting/19315)  
22 July event - [https://meetings.vtools.ieee.org/meeting\\_view/list\\_meeting/19317](https://meetings.vtools.ieee.org/meeting_view/list_meeting/19317)



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